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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/657,139 | 09/09/2003 | Shinji Ohuchi | KKH.039D2 | 1910 |

7590 04/19/2005

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| EXAMINER | |
|---|---|
| NGUYEN, DILINH P | |
| **ART UNIT** | **PAPER NUMBER** |
| 2814 | |

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/657,139 | OHUCHI ET AL. | |
| | Examiner | Art Unit | |
| | DiLinh Nguyen | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *34-38,45-47 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-38,45-47 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 34-38 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (U.S. Pat. 5,239,198) (previously applied).

Lin et al. (figs. 6-7) disclose a semiconductor device comprising:

a BGA (ball grid array) 52 type semiconductor device including a base plate 12 and a plurality of bumps 32 formed on a backside surface of the base plate; and

a CSP (chip size package) type semiconductor device mounted on an area of the backside surface of the base plate of the BGA type semiconductor device which does not have any bumps formed thereon,

the CSP type semiconductor device having a semiconductor element 50 which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals (a plurality of pads formed on the element 51 or on the chip 50) which are formed on the main surface,

wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed (figs.6- 7, column 6, lines 55 et seq.).

- Regarding claim 35, Lin et al. disclose that the plurality of terminals 51 of the CSP type semiconductor device are electrically connected to the plurality of

bumps 32 (fig. 7) via wiring patterns 16 formed on the backside surface of the base plate (fig. 6, column 6, lines 61-65).

- Regarding claim 36, Lin et al. disclose that the plurality of terminals of the CSP type semiconductor device are coupled to the wiring patterns via solder joint 51 (fig. 7).
- Regarding claim 37, Lin et al. disclose that the CSP type semiconductor device is mounted on the BGA type semiconductor device so that a front surface of the CSP type semiconductor device faces the backside surface of the base plate 12 (fig. 7).
- Regarding claim 38, Lin et al. disclose that the backside surface of the base plate is mounted to a printed circuit board 38 (column 5, line 65) via the plurality of bumps 32, and the CSP type semiconductor device as mounted on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps 32 (fig. 7).
- Regarding claim 46, Lin et al. disclose that the main surface of the semiconductor element faces the backside surface of the base plate (fig. 7).

***Claim Rejections - 35 USC § 103.***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

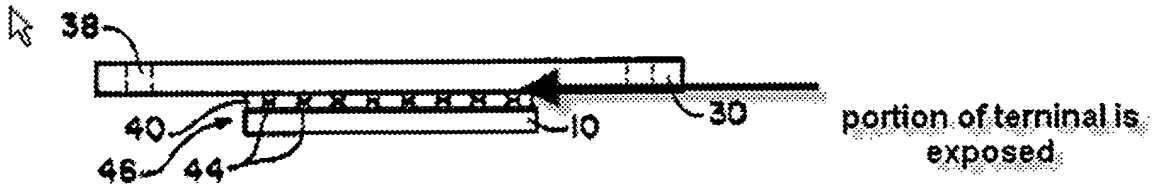
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 45-47 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. 5239198) (previously applied) in view of Schrock (U.S. Pat. 5,861,678) (previously applied).

Lin et al. fail to disclose a resin that covers the main surface of the semiconductor element and side surface of the terminals.

However, Schrock discloses a CSP type semiconductor device 10 has a resin 40 that covers the main surface of the semiconductor element and side surfaces of the terminals 44 (figs. 4a-4b, column 4, lines 33-58). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Lin et al. by having the resin layer that covers the main surface of the CSP, as taught by Schrock, for firmly secure the die to the substrate (column 5, lines 62-65).

- Regarding claim 47, Lin et al. disclose that the main surface of the semiconductor element faces the backside surface of the base plate (fig. 7).
- Regarding claim 53, Schrock discloses that the main surface of the semiconductor element 10 is sealed with a resin 40, and portion of each of the plurality of terminals are exposed from the resin 40 (cover fig.).



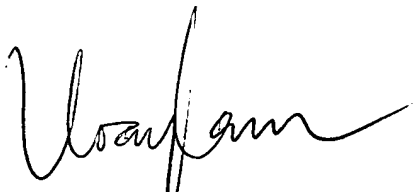
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN



HOAI PHAM
PRIMARY EXAMINER